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| 10/562,869 | 04/07/2006 | Walter Fix | 411000-144 | 6418 |

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| EXAMINER | |
|---|---|
| MONTALVO, EVA Y | |
| ART UNIT | PAPER NUMBER |
| 2814 | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/562,869 | FIX ET AL. | |
| | Examiner | Art Unit | |
| | Eva Montalvo | 2814 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *15 April 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1,3 and 8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3 and 8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12/28/2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

1. This Office action responds to the amendment filed on 04/15/2009.

### *Continued Examination Under 37 CFR 1.114*

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 4/15/2009 has been entered.

### *Drawings*

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the gate electrode of the switching FET is directly capacitively coupled to one of the source/drain electrodes of the switching FET of claim 1 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

4. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the

renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

***Specification***

5. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. In the instant case, the description fails to provide support for the gate electrode of the switching FET is directly capacitively coupled to one of the source/drain electrodes of the switching FET, as it is recited in claim 1. Appropriate correction is required. See 37 CFR 1.75 (d) (1) and MPEP § 608.01(o).

***Claim Rejections - 35 USC § 112***

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

*7.* Claim 1 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. In the instant case, the limitation the gate electrode of the switching FET is directly capacitively couple to one of the source/drain electrodes of the switching FET in claim 1, is not disclosed in drawings or written descriptions.

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 1 recites the limitation "the input" and "the output" in line 14. There is insufficient antecedent basis for this limitation in the claim.

***Claim Rejections - 35 USC § 103***

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

11. Claims 1, 3 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawamoto in view of Mutsaers (cited in previous action).

Kawamoto discloses a logic gate comprising a circuit (see fig. 2A and col. 1, line 59 to col. 2, line 13) having an output and comprising at least one charging field effect transistor (charging FET) (i.e., TL1) on a substrate; and at least one switching field effect transistor (switching FET) (i.e., TD1) having at least one gate electrode, a source electrode and a drain

electrode; the drain-source electrodes of the charging and switching transistors being arranged to be coupled in series between a voltage source and a reference potential such that the gate electrode of the charging FET is not connected via an electrical line directly to a voltage source, to the reference potential, to the input, or to the output.

Although the device disclosed by Kawamoto shows substantial features of the claimed invention, it fails to expressly teach that the FET is organic and the charging FET including a first structured layer comprising source and drain followed by a semiconductor layer on the electrodes followed by a layer of insulating material on the semiconductor layer and adjacent to and contiguous with a second electrode layer forming a gate electrode.

Nonetheless, these features are well known in the art and would have been an obvious modification of the device disclosed by Kawamoto, as evidenced by Mutsaers.

Mutsaers discloses a device comprising an organic FET (see Fig. 2) and the FET including a first structured layer (3) comprising source and drain (32 and 33) followed by a semiconductor layer (4) on the electrodes followed by a layer of insulating material (5) on the semiconductor layer and adjacent to and contiguous with a second electrode layer (6) forming a gate electrode.

Given the teachings of Mutsaers, a person having ordinary skill in the art at the time of invention would have readily recognized the desirability and advantages of modifying Kawamoto, as suggested by Mutsaers, by employing an organic FETs in the circuit. This would provide a simple and cost effect way of manufacture FETs utilized in the integrated circuits when comparing to silicon technologies (see col. 1, lines 14-28 and col. 2, lines 29-55).

12. As to claims 3 and 8, Mutsaers discloses a device, where the gate electrode of the charging FET overlapping one source/drain electrode of the charging FET (see Fig. 2); and the organic logic gate is constructed without plated-through holes (see Fig. 1 and 2). The examiner notes that Mutsaers does not disclose a logic gate constructed with plated-through holes.

***Remarks***

13. Kawamoto in view of Mutsaers shows most limitations in the claims including a charging FET (TL1), a switching FET (TD1), and the drain/source electrodes of the charging and switching FET are connected in series, such that the gate of the charging FET is not connected directed to a voltage source, reference potential, input or output. The limitation is claim 1 of the gate electrode of the switching FET is directly capacititively coupled to one of the source/drain electrodes of the switching FET is not disclosed by the prior art of record. However, said limitation fails to satisfy the written description requirement to inform a skilled artisan that the applicants were in possession of the claimed invention as a whole at the time of the application was filed. See MPEP § 2163 fro guidelines pertaining the written description requirement.

***Response to Arguments***

14. Applicant's arguments with respect to claims 1, 3 and 8 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eva Montalvo whose telephone number is (571)270-3829. The examiner can normally be reached on Monday through Thursday 7:30-5:30 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marcos D. Pizarro-Crespo can be reached on (571)272-1716. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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